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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,604	08/30/2000	Thomas J. Krutsick	5	9105

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Docket Administrator Rm 3C 512
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EXAMINER

SEFER, AHMED N

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 04/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/650,604	KRUTSICK, THOMAS J.
Examiner	Art Unit	
A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on ____ .

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-27 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .

4) Interview Summary (PTO-413) Paper No(s). ____ .
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Reference numeral 22 mentioned on pages 4 (line 6), 8 (line 21), 9 (lines 14-17) and 10 (line 1) and reference numeral 98 mentioned on page 9 (line 15). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. Claims 1, 10 and 19 are objected to because of the following informalities: The limitation "the conductors formed ..." recited in claims 1, 10 and 19 should read "the metal conductors formed ...", "a fist layer" recited in claim 19 should read "a first layer" and the limitation "the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor" recited in claims 1, 10 and 19 is not clear. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26, as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Kondo US Patent No. 4,609,935

Kondo discloses (see figs. 1-9 and col. 6, lines 13-15) an integrated circuit including a field plated resistor or a field plate resistor (as in claim 19), comprising a resistor formed in a substrate, the resistor having first and second contact regions 40; a first layer of insulative material 33 or oxide (as in claims 2, 11 and 20) over the resistor, the first layer of insulative material having a window therethrough to the first contact region; a layer of doped polysilicon 39 over the first layer of insulative material to define a field plate over the resistor, the polysilicon filling the window and making contact with the first contact region of the resistor, the field plate extending over the resistor body to proximate the second contact region; a second layer of insulative material 42 or oxide (as in claims 3, 12 and 21) over the resistor, a portion of the second layer of insulative material covering the field plate, the second layer of insulative material having a first window therethrough to the field plate and a second window therethrough to the second contact region; metal conductors 44 extending over the polysilicon field plate, the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor, or metal conductors 44 in a first layer of metal in the integrated circuit extending over the polysilicon field plate, the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor (as in claim 10).

As to claims 6, 8, 15, 17, 24 and 26 Kondo discloses a barrier layer 41 formed at a metal-polysilicon interface in the first window of the second layer of insulative material and at a metal-substrate interface in the second window of the second layer of insulative material (as in claims 8, 17 and 26).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-3, 10-12 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuyama et al (JP 57-100723) in view of Tamagawa US Patent No. 6,046,491.

Mitsuyama et al disclose in figs. 7-9 an integrated circuit including a field plated resistor, comprising a resistor formed in a substrate, the resistor having first and second contact regions 3, 3': a first layer of insulative material 4 or oxide (as in claims 2, 11 and 20) over the resistor, the first layer of insulative material having a window therethrough to the first contact region; a layer of doped polysilicon over the first layer of insulative material to define a field plate over the resistor, the polysilicon filling the window and making contact with the first contact region of the resistor, the field plate extending over the resistor body to proximate the second contact region; a second layer of insulative material 4' or oxide (as in claims 3, 12 and 21) over the resistor, a portion

of the second layer of insulative material covering the field plate, the second layer of insulative material having a first window therethrough to the field plate and a second window therethrough to the second contact region; a metal conductor extending over the polysilicon field plate.

Tamagawa discloses in fig. 7, metal conductors 19 extending over the polysilicon field plate 21, the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor, or metal conductors 21 in a first layer of metal in the integrated circuit extending over the polysilicon field plate, the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor (as in claim 10).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Tamagawa with the device of Mitsuyama et al, since that would provide the necessary wiring.

7. Claims 4, 6, 13, 15, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Pfiester US Patent No. 4,948,747.

Kondo discloses all the claimed subject matter but does not disclose an insulative spacer formed around a field plate.

Pfiester discloses in fig. 7 an insulative spacer formed around a field plate; a barrier layer 32 formed at a metal-polysilicon layer interface.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use an insulative spacer around a field plate, since that would provide a protection to a resistor portion. It would have been obvious to use a barrier

layer at metal-polysilicon layer interface (as in claims 6, 15 and 24), since that would provide the required conductivity for the interconnection.

8. Claims 4, 13 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Tsuji US Patent No. 5,804,857.

Kondo discloses all the claimed subject matter but does not disclose an insulative spacer formed around a field plate.

Tsuji discloses in figs. 2 and 4 an insulative spacer 19 formed around a field plate.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use an insulative spacer around a field plate, since that would provide a protection to a resistor portion.

9. Claims 5, 14 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Tanaka et al. (JP 1 – 130552).

Kondo discloses all the claimed subject matter but does not disclose an enhanced contact region at a polysilicon-substrate interface.

Tanaka et al disclose in fig. 1 an enhanced contact region formed at a polysilicon-substrate interface.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use an enhanced contact region, since that would provide the device an excellent resistance characteristics.

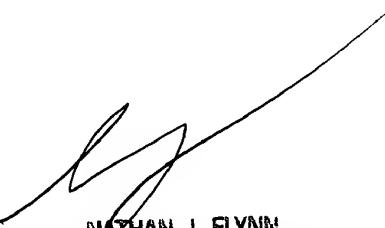
10. Claims 7, 9, 16, 18, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo.

Kondo teaches a first barrier layer formed at different interfaces of the device, but does not specifically teach the formation of a second barrier layer at a metal-first barrier layer interface. It would have been obvious to one having ordinary skill in the art at the time the invention was made to partition the first barrier layer to form a second barrier layer at a metal-first barrier layer interface, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bermis Co., 193 USPQ8.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
April 21, 2002



NATHAN J. FLYNN
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